# Two dimensional numerical simulations of 1/f noise by GR mechanisms in thin film transistors: Effects of induced defect technology

Abdelmalek Boukhenoufa, Laurent Pichon, Christophe Cordier

# Two dimensional numerical simulations of 1/f noise by GR mechanisms in thin film transistors: Effects of induced defect technology

A. Boukhenoufa[a], L. Pichon[b,*], C. Cordier[a]

[a]*GREYC, CNRS UMR 6072, ENSICAEN-Université de Caen, 6 bd du Maréchal Juin, 14050 Caen, France,*
[b]*GM-IETR, CNRS UMR 6164, campus de beaulieu, avenue du général Leclerc, 35042 Rennes, France*

**Abstract**

Two dimensional (2D) numerical simulation of low-frequency (1/f) noise is carried out in N-channel polysilicon thin film transistors biased from weak to strong inversion. Noise is simulated by Generation-Recombination processes. Simulation is based on the impedance field method of Shockley. A 2D analysis of the local noise level shows that contribution at grain boundaries dominates from weak to strong inversion. 1/f noise level in the bulk of the active layer is higher when devices are biased in the weak inversion. In the strong inversion contribution of sources close to the interface dominates.

## 1. Introduction

Polysilicon thin-film transistors (TFTs) are key elements for large area electronics such as flat panel displays, and flexible electronics because of their high potential usefulness in driving circuits and/or in addressing pixels.

Some improvements remain in TFT technology because the electrical properties are strongly affected by the trapping of carriers at the defects located at the grain boundaries and at the oxide/semiconductor interface. In particular the high level of low frequency (1/f) noise is one limiting factor for using such devices [1].

The physical origin of 1/f noise in TFTs due to carrier fluctuation is still controversial. It is useful to model 1/f noise by trapping/detrapping (T/D) of carriers into slow oxide traps [2-3]. However, generation/recombination (GR) processes of carriers at grain boundaries (GBs) have been previously suggested [2], and the corresponding defect densities can be deduced. 1/f noise level is then strongly dependent on both interface and active layer qualities, and thus on fabrication process parameters [3,4].

Corresponding author : lpichon@univ-rennes1.fr,
Tel (33)2 23 23 56 65, Fax: (33)2 23 23 56 71

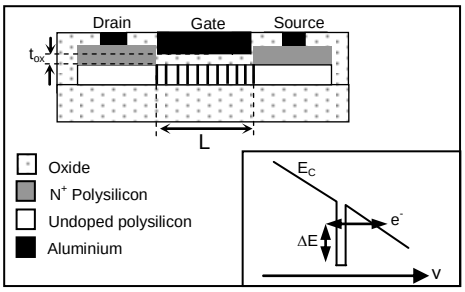



Figure 1. Cross section of the device for 2D simulation of TFT. W/L=50µm/20µm. Inset: schematic thermally assisted tunnelling process at GBs.

A good understanding of transport characteristics such as noise is necessary to improve device modelling and TFT technologies. In the paper we report the study of the two dimensional (2D) spatial distribution of the 1/f local noise level, simulated by GR processes within the bulk of N-Channel TFTs. Simulation of devices is based on structures issued from low temperature (≤600°C) technology. TFTs are built with a single solid phase crystallized polysilicon layer (figure 1 (a)): the upper part is heavily doped (source and drain regions) and the bottom part is none intentionally doped (active layer). More details for fabrication are given in ref [5]. The impact of the structural defects, induced by the technology, on the noise level is analyzed.

## 2. Simulation

In the simulated TFTs (fig. 1) the doped and undoped polycrystalline films are 150 nm thick. The oxide thickness $t_{ox}$ is 60 nm. The polysilicon is described by introducing equally spaced GBs, depicted as thin amorphous silicon layer with a width of 2 nm, perpendicular to the carrier transit direction. The grain size is 300 nm. Geometrical dimensions of each part of the structure correspond to TFTs previously processed and electrically studied (see ref [5]). The corresponding transfer characteristic measured in the linear mode is plotted in the figure 2 (a).

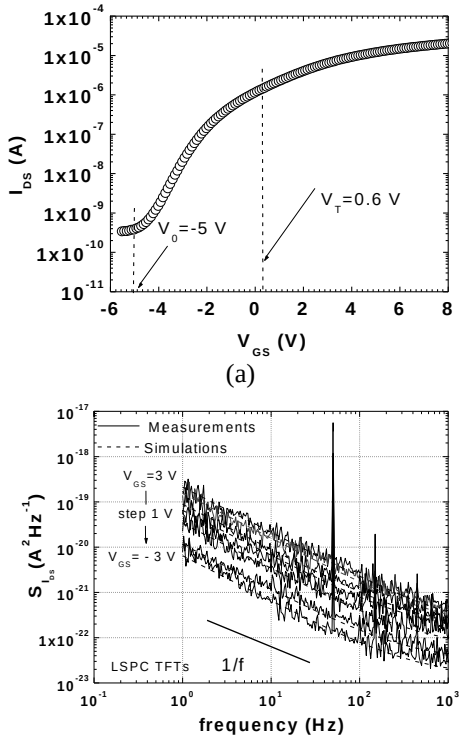



Figure 2 (a) Experimental transfer characteristics in the linear mode ($V_{DS}$=300V) of the simulated TFTs. $V_T$ is the threshold voltage and $V_0$ is identified to the flatband voltage. (b) Experimental and simulated noise current spectra in TFT biased from weak to strong inversion (-3V≤$V_{GS}$≤3V).

Low frequency noise was simulated for TFTs biased from the weak to the strong inversion and operating in the linear mode ($V_{DS}$=300mV) by using the DESSIS-ISE multi-dimensional simulator of ISE-TCAD software [6]. The noise simulation is based on the impedance field method (IFM) of Shockley [7,8]. A numerically efficient Green function approach to the Langevin equation-based simulation of the IFM is the basis for the implementation in ISE simulator. The complex (Fourier-transformed) Green functions G describe the propagation of perturbations inside the device to the contacts. According to the definition of the IFM, the two dimensional spatial distribution of the numerical simulation of the local noise voltage spectral density (2D-LNVSD) in the bulk of polysilicon layers was calculated from integration over all noise sources [6]:

$$S(\omega, r) = \sum_{\alpha=n,p} \int_{\Omega} G_\alpha K^{GR}_{\alpha,\alpha} G^*_\alpha dr + \sum_{\alpha=n,p} \int_{\Omega} G_\alpha K^{fGR}_{\alpha,\alpha} G^*_\alpha dr \quad (1)$$

where n and p refer respectively to electrons and holes, $K^{GR}$, $K^{fGR}$ and $\Omega$ represent the GR local noise source, the flicker GR local noise source and the device volume respectively.

The GR noise source model that we have chosen is expressed as a tensor:

$$K^{GR}_{n,n} = \frac{J_n \otimes J_n}{n} \frac{4\alpha_{gr}\tau_{gr}}{1+\omega^2\tau_{gr}^2} \quad (2)$$

where $J_n$ is the local current density, n is the local carrier density, $\tau_{eq}$ is the equivalent GR lifetime, $\alpha_{gr}$ is a constant which represents the quasi Poissonian character of the carrier number (N) fluctuations ($<\Delta N^2>=\alpha_{gr}<N>$) and $\omega=2\pi f$ is the angular frequency.

The 1/f noise source is represented as the sum of GR noises produced by sub bands of impurities or defects, with a corresponding continuous distribution of relaxation times between $\tau_1$ and $\tau_2$: $g(\tau) = (\ln(\tau_2/\tau_1)\tau)^{-1}$ [9]. The flicker GR local noise source is then expressed as a tensor:

$$K^{fGR}_{n,n} = \frac{J_n \otimes J_n}{n} \frac{2\alpha_H}{\pi f \log(\frac{\tau_2}{\tau_1})} [\arctan(\omega\tau_2) - \arctan(\omega\tau_1)] \quad (3)$$

$\alpha_H$ is identified to *the microscopic Hooge noise parameter* associated with the local source of noise. $\tau_1$ and $\tau_2$ are chosen such that $1/\tau_2 << \omega << 1/\tau_1$.

The calculation of the drain current noise spectral density with the classical form of IFM according to (1) requires the knowledge of the local noise source K. We defined the flicker GR local noise sources $K^{fGR}$ within the active layer following (3) with $\alpha_H$ assumed identical for all sources. In order to obtain a 1/f behaviour in the studied frequency band (1Hz-$10^3$Hz, see fig. 2 (b)), the relaxation times $\tau_1$ and $\tau_2$ are fixed at $10^{-7}$s and $10^4$s, respectively. High $\tau$-values are associated to slow mechanisms: i) for T/D at $SiO_2$/Sipoly interface $\tau=\tau_0\exp(\gamma y)\sim 10$ with $\tau_0\sim 10^{-12}$s, $\gamma\sim 10^{10}$m$^{-1}$, y=3nm the oxide tunnel depth [9], ii) for GR at GBs associated to thermally assisted tunnelling process (see inset of fig. 1) $\tau=\tau_0\exp(\Delta E/kT)\exp(\gamma y)$ [10] and thus a so high $\tau_2=10^4$ could be justified with $y\approx 3$nm and $\Delta E\approx 0.2$eV. For some spectrums which contain a Lorentzian, we introduced a GR local noise source $K^{GR}$ given by (2).

## 3. Results and discussion

A good fit of numerical simulations with experimental 1/f noise spectrum was obtained (figure 2. (b)). Values of $\alpha_H$ versus effective voltage ($V_{GS}$ - $V_0$, $V_0$ flatband voltage), are then reported in the figure 3 (a) for devices biased from weak to strong inversion. Plot of the macroscopic apparent noise parameter $\alpha_{app}$, deduced from the experimental measurements according to the Hooge formula $S_{IDS}/I^2_{DS} = \alpha_{app}/(fN)$ with N the free carrier number in the channel, is also reported. Results show that $\alpha_H$ and $\alpha_{app}$ exhibit the same singular behaviour previously reported for $\alpha_{app}$ in ref [11], suggesting these noise parameters directly related. The higher values of $\alpha_{app}$ can be explained by the current crowding due to structural defects inducing non conducting spots described as follow.

Trapping carriers at interfacial defects such as grain boundaries induce intergranular energy barrier modelled by non conducting area between two consecutive crystalline grains (see figure 3(b)). If the restricted conducting contact region is considered to be circular then [12]:

$$\alpha_{app} = \alpha_H \frac{L^3}{20\pi a^3} \quad (4)$$

with L and a standing for the grain and the conducting spot contact sizes respectively. For homogeneous materials $\alpha_H/\alpha_{app}\sim 1$ whereas for disordered materials $\alpha_H/\alpha_{app} << 1$. This ratio can be considered as a quality factor of the polycrystalline silicon and thus as an indicator on the reliability of the TFTs.

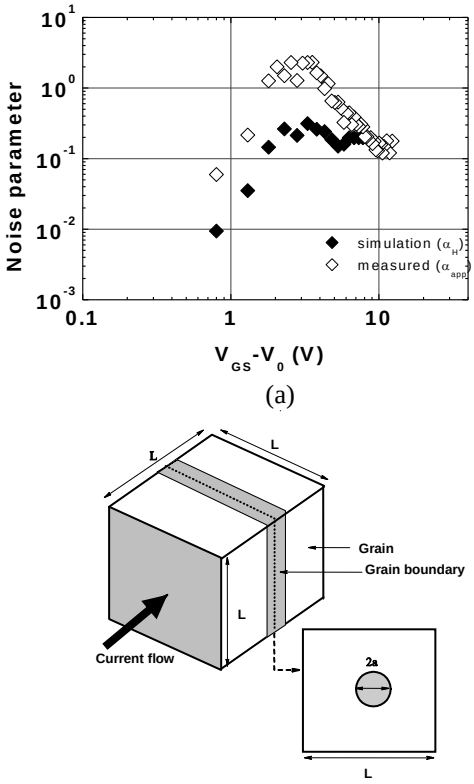



Figure 3 : (a) Noise parameters versus effective gate voltage. (b) Schematic conducting spot at GB in circular grey area.

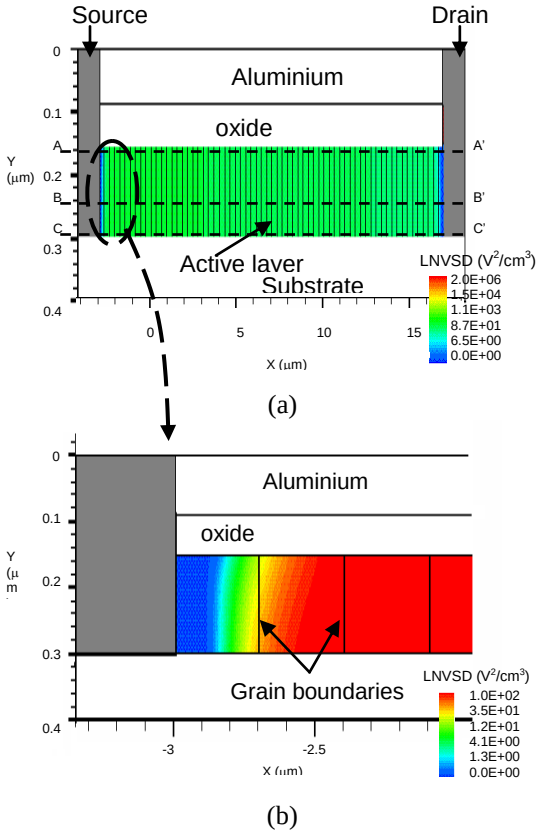



Figure 4. (a) 2D-LNSVD in the simulated TFT biased in the weak inversion ($V_{GS}$=-1V) at f=1Hz. (b) Zoom of the LNVSD close to the source region.

It is commonly admitted that the drain current is strongly controlled by intergranular energy barriers [3]. At low gate voltages (from weak to moderate inversion) energy barriers are maximum, then the current flows preferentially the lowest barriers in restricted contacts regions at GBs and then $\alpha_{app}>\alpha_H$. At high gate voltages (from weak to strong inversion) the energy barriers decrease, the current density becomes uniform and then $\alpha_{app}\sim\alpha_H$. In our case the maximum value of this ratio is ~0.17.

The 2D-LNVSD within the active layer of the device biased in the weak inversion ($V_{GS}$=-1V see fig. 2 (a)) is displayed in the figure 4. Results show that the local noise magnitude is uniform within the intragranular bulk of the active layer, and that it is higher at GBs. The lower noise level close to the source/drain regions observed in the figure 4 (b) is explained because of the higher local carrier concentration in these regions resulting, according to (3), to a lower local noise spectral density. For TFTs biased in the strong inversion (with $V_{GS}$=5V, see fig. 2 (a)) contribution of sources of noise close to the interface dominates (fig. 5): noise level increases over one decade from the bulk of the active layer to the interface, with a quasi non existing contribution of the sources at the back (Si-poly/substrate) interface. This shows that the local noise in the TFTs biased in the strong inversion is mainly located close to the interface. This result is in contrast for devices biased in the weak inversion: all local sources within the active layer uniformly contribute to noise with a higher magnitude (fig. 4), and then the noise rules over the whole bulk of the active layer. Furthermore, the higher local noise magnitude in devices biased in the weak inversion will be further discussed in

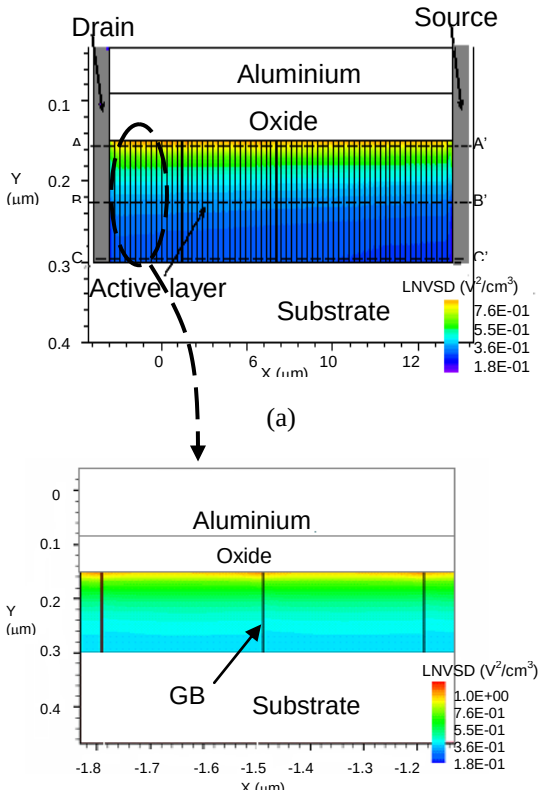



Figure 5. 2D-LNVSD in the simulated TFT biased in the strong inversion ($V_{GS}$=5V) at f=1Hz. (b) Zoom of the LNVSD close to the source region.

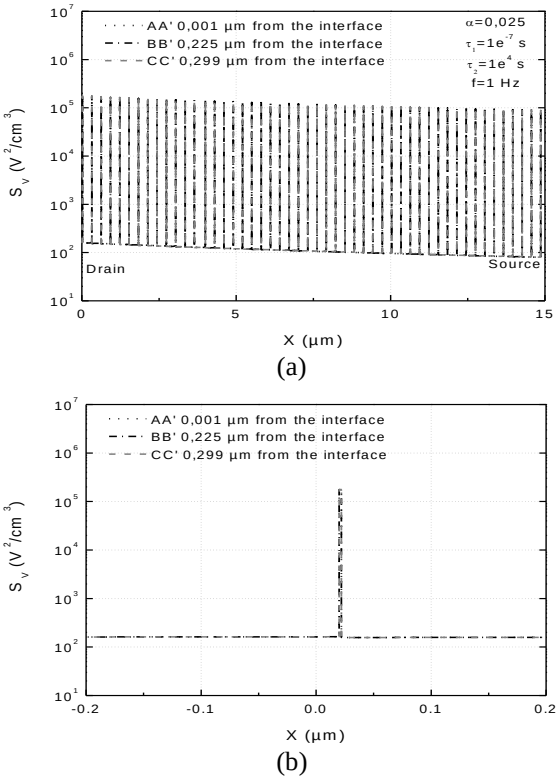



Figure 6: (a) Distribution from the source to the drain, for tree distances from the gate insulator/active layer interface, of the local noise level in the simulated device biased in the weak inversion ($V_{GS}$=-1V) at f=1Hz. (b) Zoom of the distribution of the noise.

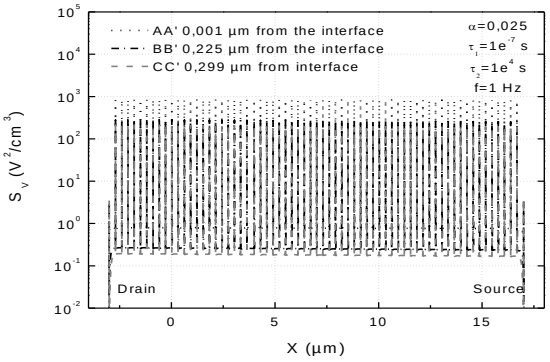
relation to the macroscopic noise level deduced from measurements.

The impact of the contribution of the GBs is depicted in the figures 6 and 7. A very high contribution of the sources of noise located at the grain boundaries is observed. LNVSD is 3 decades higher at the GBs than in the intragrain region. For devices biased in the strong inversion, it increases both at the grain boundaries and within the grains as the distance from the bulk of the active layer to the gate oxide/active layer interface decreases. All these results suggest a high contribution of the local sources associated with defects located at the interfaces (ie at GBs and along the $SiO_2$/Si-poly interface). Then it underlines the preponderant role previously reported of these defects on the macroscopic 1/f noise level in the TFTs [2.3].

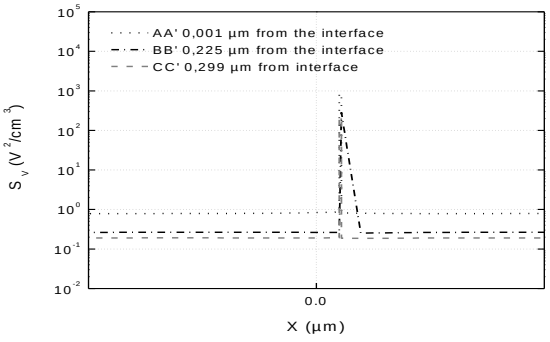
The higher level of the local (or microscopic) noise previously mentioned in TFTs biased in the weak inversion can be related to the macroscopic model following:

$$\begin{cases} g_d = \dfrac{I_{DS}}{V_{DS}} \\ S_{I_{DS}} = g_d^2 S_{V_{DS}} \end{cases} \Rightarrow \quad S_{V_{DS}} = \frac{S_{I_{DS}}}{I_{DS}^2} V_{DS}^2 \qquad (5)$$

where $g_d$ is the channel conductance, $S_{IDS}$ and $S_{VDS}$ are respectively the drain current and the voltage noise spectra. Then, as displayed in the fig. 3 (a) in ref[3], at a fixed $V_{DS}$, $S_{VDS}$ decreases from weak to strong inversion according to the plot of $S_{I_{DS}} / I_{DS}^2$ versus $I_{DS}$. The ratio of $S_{I_{DS}} / I_{DS}^2$ values measured at $V_{GS}$=-1V and $V_{GS}$=5V respectively is ~$10^2$. For our




(a)




(b)

Figure 7. (a) Distribution from the source to the drain, for tree distances from the gate insulator/active layer interface, of the local noise level in the simulated device biased in the strong inversion ($V_{GS}$=5V) at f=1Hz. (b) Zoom of the distribution of the noise.

simulated results the maximum value of the LNVSD (at GBs) in the weak inversion is ~$10^5$, whereas in the strong inversion it is ~$10^3$, then it agrees with the ratio of the measured $S_{I\,DS} / I_{DS}^2$ from weak to strong inversion.

## 4. Conclusion

2D Numerical simulation of low frequency noise in TFTs is first presented. Noise is modelled by carrier fluctuations due to GR mechanisms of carriers and local sources of noise are uniformly distributed within the active layer. The effects of the induced defect technology (grain boundaries and gate insulator/active layer) on the 1/f noise level are pointed out. Results show that the low frequency noise in TFTs can be a criterion on the quality of the polycrystalline silicon and of the interface. Furthermore, the study shows that GR mechanisms, in particular at the grain boundaries, have to be more considered to improve TFT numerical simulation noise model to predict the reliability of the TFTs in relation with the technology.

## References


[1] M. Aoki, T. Hashimoto, T. Yamanaka, T. Nagano, Jap. J. Appl. Phys. **35**(1996) 838.

[2] C.A. Dimitriadis, G. Kamarinos, J. Brini, IEEE Elect. Dev. Lett. **22**(2001) 381.

[3] L. Pichon, A. Boukhenoufa, C. Cordier, B. Cretu, J. Appl. Phys. **100**(2006) 54504.

[4] A. Mercha, L. Pichon, R. Carin, K. Mourgues, O. Bonnaud, Thin Solid Films **383**(2001) 303.

[5] L.Pichon, K. Mourgues, F. Raoult, T. Mohammed-Brahim, K. Kis-Sion, D. Briand, O. Bonnaud, *Semicond. Sci. Technol.*, **16**(2001) 918

[6] DESSIS-ISE, ISE-TCAD Release 8.5, User's Manual, Zurich, 2004.

[7] W. Shockley, J. A. Copeland, R. P. James, Quantum theory of atoms, molecules and the solid state. Ed P. O. Lowdin. Academic, New York, 1966

[8] F. Bonani, G. Ghione, M. R. Pinto, R. K. Smith, IEEE Trans. Electron. Dev. **45**(1998) 261.

[9] S. Christensson, I. Lundström, C. Svensson, *Sol. Stat. Elect.*, 11, pp 797-812, 1968

[10] G. Vincent, A. Chantre, D. Bois, J. Appl. Phys. **50**, **N°8**,(1979) 5484.

[11] A. Boukhenoufa, C. Cordier, L. Pichon, B. Cretu, to be published in Thin Solid Films.

[12] A. Mercha, L.K. J. Vandamme, L. Pichon, R. Carin, J. Appl. Phys. **90(8)**, (2001) 4019